CLAIMS

What is claimed is:

1. A memory cell array comprising:

a two dimensional array of memory cells fabricated on a semiconductor substrate the memory cells arranged in a plurality of rows of memory cells defining a horizontal row direction and a plurality columns of memory cells defining a column direction that is perpendicular to the horizontal row direction;

each column of memory cells comprising a plurality of channel regions of the substrate, each channel region of the substrate being separated from an adjacent channel region within the column by a source/drain region, each source drain region being a portion of the substrate that is implanted with a first impurity to form a first conductivity type semiconductor;

a plurality of conductive interconnects, each conductive interconnect being positioned above only one source/drain region within a first column of the memory cells and coupling to only one other source/drain region, the one other source/drain region begin in a second column that is adjacent to the first column and being in the same row as the source/drain region, and wherein the conductive interconnects are positioned such that every other conductive interconnect connects to the second source drain region in the adjacent column to a right side of the first column and every other interconnect connects to the second source drain region inn the adjacent column to the left side of the first column; and

a plurality of source/drain control lines, extending above the array in the column direction and positioned between adjacent columns of memory cells and electrically coupling to each conductive interconnect that couples between a source/drain region in each of the adjacent columns.

2. The memory cell array of claim 1, further comprising:

a charge storage cell positioned above each channel region:

a plurality of conductive word lines, each conductive word line extending across the top of each charge storage cell within a row of memory cells and forming a gate electrode over each charge storage region within the row of memory cells.

3. The memory cell array of claim 2, wherein:

each of the source/drain control lines is spaced apart from each conductive interconnect; and

the array further includes a plurality of conductive vias, each conductive via extending from a source/drain control line to only one of the plurality of interconnects.

4. The memory cell array of claim 3, wherein:

The source/drain control lines are positioned above the word lines, and isolated from the word lines; and

each conductive via extends from the source/drain control line downward to the one of the plurality of interconnects between, and isolated from, adjacent word lines.

5. The memory cell array of claim 4, wherein:

each column of memory cells is separated from the adjacent column of memory cells by an insulator channel region within the substrate, the insulator channel region defining sides, in the horizontal direction, of each source/drain region and each channel region within the column of memory cells.

6. The memory cell array of claim 5, wherein:

each charge storage cell is a floating gate charge storage cell comprising:

a tunnel dielectric layer adjacent to the channel region;

a top dielectric layer adjacent to the word lines; and

a conductive gate positioned between the tunnel dielectric layer and the top dielectric layer.

7. The memory cell array of claim 5, wherein:

each charge storage cell is a charge trapping dielectric charge storage cell comprising:

a tunnel dielectric layer adjacent to the channel region;

a top dielectric layer adjacent to the word lines; and

a charge trapping dielectric positioned between the tunnel dielectric layer and the top dielectric layer.

8. A memory cell array comprising:

a two dimensional array of memory cells fabricated on a semiconductor substrate the memory cells arranged in a plurality of rows of memory cells defining a horizontal row direction and a plurality columns of memory cells defining a column direction that is perpendicular to the horizontal row direction;

each column of memory cells comprising a plurality of channel regions of the substrate, each channel region of the substrate being separated from an adjacent channel region within the column by a source/drain region, each source drain region being a portion of the substrate that is implanted with a first impurity to form a first conductivity type semiconductor;

a plurality of conductive interconnects, each conductive interconnect being positioned above only one source/drain region within the column of memory cells and couples to only one other source/drain region, the one other source/drain region begin in a second column that is adjacent to the column and being in the same row as the source/drain region, and wherein the conductive interconnects are positioned such that a conductive interconnect is position above only every second source/drain region within a first column of memory cells and every second conductive interconnect within the first column of memory cells connects to the second source drain region in the adjacent column to a right side of the first column and every other interconnect connects to the second source drain region inn the adjacent column to the left side of the first column; and

a plurality of source/drain control lines, extending above the array in the column direction and positioned between adjacent columns of memory cells and electrically coupling to each conductive interconnect that couples between a source/drain region in each of the adjacent columns.

9. The memory cell array of claim 8, further comprising:

a charge storage cell positioned above each channel region:

a plurality of conductive word lines, each conductive word line extending across the top of each charge storage cell within a row of memory cells and forming a gate electrode over each charge storage region within the row of memory cells.

10. The memory cell array of claim 9, wherein:

each of the source/drain control lines is spaced apart from each conductive interconnect; and

the array further includes a plurality of conductive vias, each conductive via extending from a source/drain control line to only one of the plurality of interconnects.

11. The memory cell array of claim 10, wherein:

The source/drain control lines are positioned above the word lines, and isolated from the word lines; and

each conductive via extends from the source/drain control line downward to the one of the plurality of interconnects between, and isolated from, adjacent word lines.

12. The memory cell array of claim 11, wherein:

each column of memory cells is separated from the adjacent column of memory cells by an insulator channel region within the substrate, the insulator channel region defining sides, in the horizontal direction, of each source/drain region and each channel region within the column of memory cells.

13. The memory cell array of claim 12, wherein:

each charge storage cell is a floating gate charge storage cell comprising:

a tunnel dielectric layer adjacent to the channel region;

a top dielectric layer adjacent to the word lines; and

a conductive gate positioned between the tunnel dielectric layer and the top dielectric layer.

14. The memory cell array of claim 12, wherein:

each charge storage cell is a charge trapping dielectric charge storage cell comprising:

a tunnel dielectric layer adjacent to the channel region;

a top dielectric layer adjacent to the word lines; and

a charge trapping dielectric positioned between the tunnel dielectric layer and the top dielectric layer.

15. A memory cell array comprising:

a two dimensional array of memory cells fabricated on a semiconductor substrate the memory cells arranged in a plurality of rows of memory cells defining a horizontal row direction and a plurality columns of memory cells defining a column direction that is perpendicular to the horizontal row direction;

a plurality of insulator channels within the semiconductor substrate that extend in the column direction, each insulator channel extending between two adjacent columns of memory cells;

a plurality of generally rectangular channel regions within the semiconductor substrate, each channel region extending in the horizontal row direction between two of the insulator channels that are on opposing sides of the channel region and extending in the column direction by two semiconductor junctions, each semiconductor junction being a junction with a source/drain implant region of the substrate which is adjacent to, and on opposing sides of, the channel region;

a charge storage cell positioned above each channel region;

a plurality of word lines, each word line extending across the top of each charge storage cell within a row of memory cells and forming a gate electrode over each charge storage region within the row of memory cells; and

a plurality of source/drain control lines, extending in the column direction between columns of memory cells and interconnecting to a plurality of conductive interconnects, wherein the plurality of interconnects are each coupled to only one source/drain control line and are arranged in a staggered pattern such that each source/drain region couples to only one interconnect and such that the two source/drain regions on opposing sides of each channel region, in the column direction, are each coupled by one of the conductive interconnects to separate and adjacent source drain control lines.

16. The memory cell array of claim 15, wherein:

each of the source/drain control lines is spaced apart from each conductive interconnect; and

the array further includes a plurality of conductive vias, each conductive via extending from a source/drain control line to only one of the plurality of interconnects.

17. The memory cell array of claim 16, wherein:

The source/drain control lines are positioned above the word lines, and isolated from the word lines; and

each conductive via extends from the source/drain control line downward to the one of the plurality of interconnects between, and isolated from, adjacent word lines.

18. The memory cell array of claim 17, wherein:

each charge storage cell is a floating gate charge storage cell comprising:

a tunnel dielectric layer adjacent to the channel region;

a top dielectric layer adjacent to the word lines; and

a conductive gate positioned between the tunnel dielectric layer and the top dielectric layer.

19. The memory cell array of claim 17, wherein:

each charge storage cell is a charge trapping dielectric charge storage cell comprising:

a tunnel dielectric layer adjacent to the channel region;

a top dielectric layer adjacent to the word lines; and

a charge trapping dielectric positioned between the tunnel dielectric layer and the top dielectric layer.

20. A memory cell array comprising:

a two dimensional array of memory cells fabricated on a semiconductor substrate the memory cells arranged in a plurality of rows of memory cells defining a horizontal row direction and a plurality columns of memory cells defining a column direction that is perpendicular to the horizontal row direction;

a plurality of insulator channels within the semiconductor substrate that extend in the column direction, each insulator channel extending between two adjacent columns of memory cells;

a plurality of generally rectangular channel regions within the semiconductor substrate, each channel region extending in the horizontal row direction between two of the insulator channels that are on opposing sides of the channel region and extending in the column direction between two semiconductor junctions, each semiconductor junction being a junction with a source/drain implant region of the substrate which is adjacent to, and on opposing sides of, the channel region;

a charge storage cell positioned above each channel region;

a plurality of word lines, each word line extending across the top of each charge storage cell within a row of memory cells and forming a gate electrode over each charge storage region within the row of memory cells; and

a plurality of source/drain control lines, extending in the column direction between columns of memory cells and interconnecting to a plurality of conductive interconnects, wherein the plurality of interconnects are each coupled to only one source/drain control line and are arranged in a staggered pattern such that only every second source/drain region within a column couples to only one interconnect and such that:

the two source/drain regions on opposing sides of two adjacent channel regions within a column are each coupled one of the conductive interconnects to separate and adjacent source drain control lines; and

a source/drain region between the two channel regions is isolated from all of the conductive interconnects.

21. The memory cell array of claim 20, wherein:

each of the source/drain control lines is spaced apart from each conductive interconnect; and

the array further includes a plurality of conductive vias, each conductive via extending from a source/drain control line to only one of the plurality of interconnects.

22. The memory cell array of claim 21, wherein:

The source/drain control lines are positioned above the word lines, and isolated from the word lines; and

each conductive via extends from the source/drain control line downward to the one of the plurality of interconnects between, and isolated from, adjacent word lines.

23. The memory cell array of claim 22, wherein:

each charge storage cell is a floating gate charge storage cell comprising:

a tunnel dielectric layer adjacent to the channel region;

a top dielectric layer adjacent to the word lines; and

a conductive gate positioned between the tunnel dielectric layer and the top dielectric layer.

24. The memory cell array of claim 22, wherein:

each charge storage cell is a charge trapping dielectric charge storage cell comprising:

a tunnel dielectric layer adjacent to the channel region;

a top dielectric layer adjacent to the word lines; and

a charge trapping dielectric positioned between the tunnel dielectric layer and the top dielectric layer.